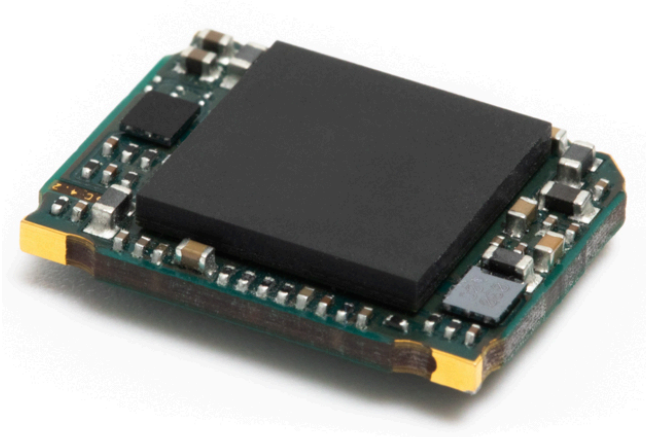
periCORE

periCORE Enhanced Connectivity via RMII



Application Note

Perinet
Seamless IoT Connectivity

Abstract

A periCORE based product can take advantage of the available media independent interface (RMII) to enhance network connectivity. This application note shows with the example of a 10BASE-T1L Phy (ADIN1100) how to connect the periCORE communication module to further Ethernet based physical devices. Hardware and software topics are handled in this document.

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Contents

1 Introduction

The periCORE communication module is equipped with 3 ports for Ethernet connectivity. Those ports are provided as media dependent interfaces (MDI) for 100BASE-T1 or 100BASE-TX, when configured. In addition to that, the periCORE does also provide one network port (PORT8) with a media independent interface MII. As shown in Figure 1, the periCORE supports the interface type RMII or SGMII.

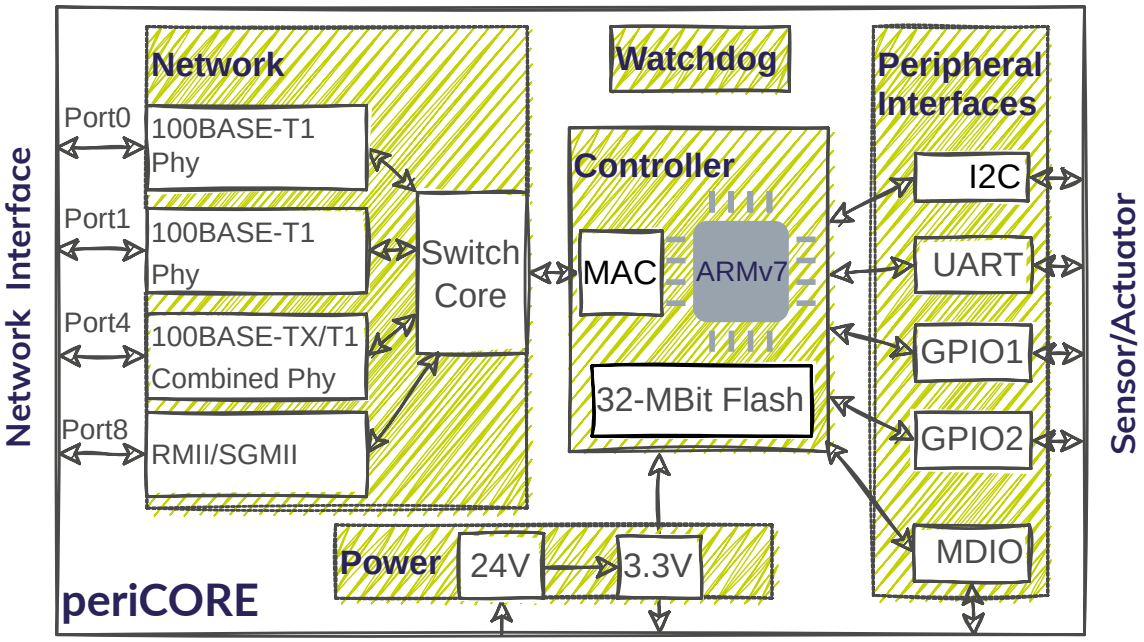

Figure 1: Block diagram of the periCORE module with its interfaces.

In this application note, the periCORE is enhanced with the connectivity to a 10BASE-T1L physical layer via the RMII on PORT8. It will present a setup where the periCORE communicates with another device over a 10BASE-T1L link.

10BASE-T1L is a physical layer Ethernet standard (IEEE 802.3cg-2019)[9], from the SPE (Single Pair Ethernet) family of standards. When compared with the previous Ethernet standards, it tries to solve their limitations with respect to cabling, distance, bandwidth and power. 10BASE-T1L is a full duplex, DC balanced and point-to-point communication scheme where the signal is modulated using PAM 3 modulation scheme with 4B3T encoding with the signalling rate of 7.5 MBaud.

In order to connect the periCORE module to the 10BASE-T1L physical layer, an external Ethernet Phy is needed and attached with RMII [10]. This document uses the ADIN1100 [2] from Analog Devices as an external Ethernet Phy. The ADIN1100 is provided on an evaluation board, EVAL-ADIN1100EBZ [1]. The setup needs the following parts:

1. periCORE Development Board [4]
2. ADIN1100 evaluation boards (EVAL-ADIN1100EBZ) [1]

More information about the periCORE module and the periCORE Development Board can be found in [3] and [5], respectively. The documentation about the ADIN1100 and EVAL-ADIN1100EBZ is available from the Analog Devices webpage [1].

2 Hardware Setup

This section explains how to prepare the hardware setup where the periCORE module communicates over a 10BASE-T1L link.

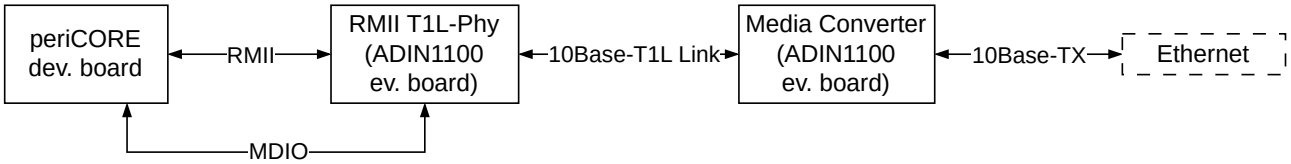

Figure 2: 10BASE-T1L test setup

The setup is sketched in Figure 2. The periCORE is connected with the Reduced media-independent interface (RMII) towards the 10BASE-T1L Phy (ADIN1100). In addition, the both are also connected via a Management Data Input/Output (MDIO) interface for configuration and management of the ADIN1100.

The periCORE communicates via 10BASE-T1L to a media converter. The media converter is another instance of the ADIN1100 evaluation board. It is configured as media converter between 10BASE-T1L and 10BASE-TX and can be accessed via most office Ethernet switches.

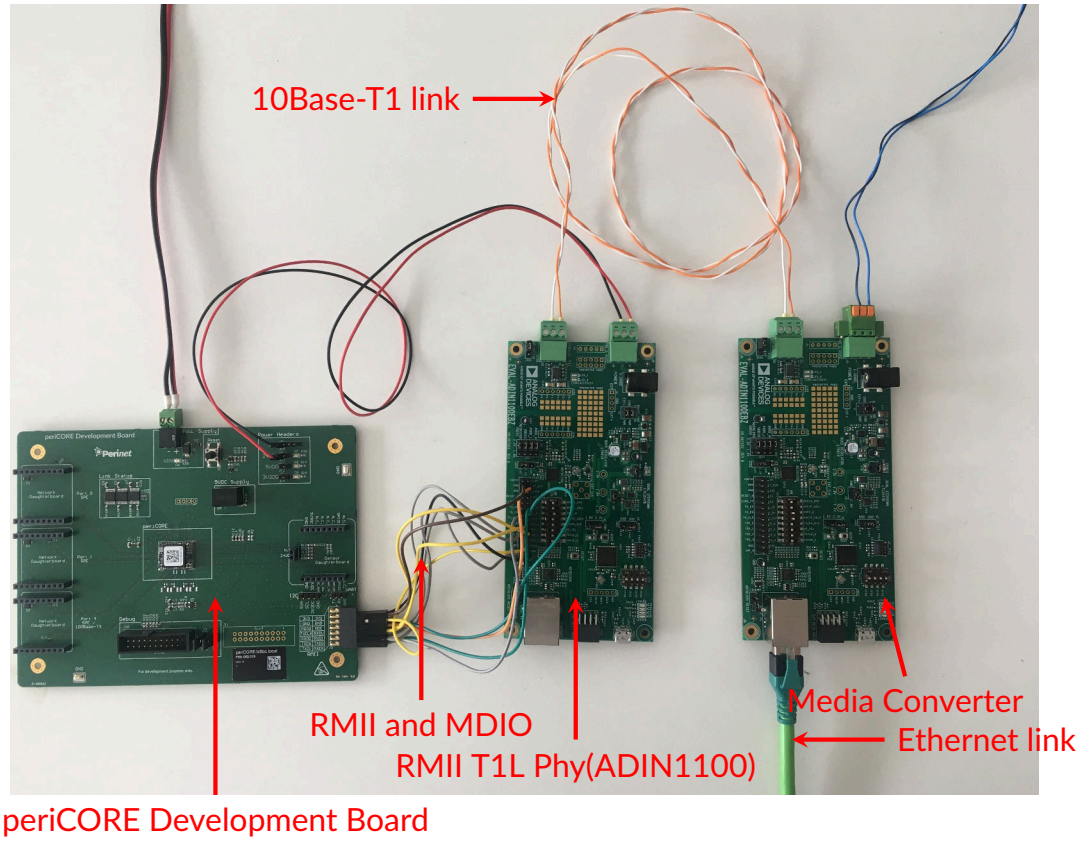

Figure 3: Hardware setup overview

2.1 RMII T1L-Phy - Patching ADIN1100 Evaluation Board

RMII uses a reference clock of 50 MHz for synchronization between the MAC and the Ethernet Phy. The periCORE communication module is not able to source this clock, but the ADIN1100 evaluation board is, although some patching needs to be done. Namely, a few additional component need to be soldered and a few components to be removed. The following changes are needed on the ADIN1100 evaluation board:

- `Y502` is a quartz oscillator for generating 50 MHz clock signal. This part should be soldered since the board comes with this part not populated. It is recommended to use SG-8101CG5.000000MHZTCHPA-ND, however, in this application note, a quartz oscillator with similar characteristics will be used: SIT8918AA-11-33S-50.000000G.
- `R203` - 0R resistor must be soldered
- `R205` - 0R resistor must be removed
- `R204` - 0R resistor must be removed

`Y502`, `R203`, `R204` and `R205` are marked in Figure 4.

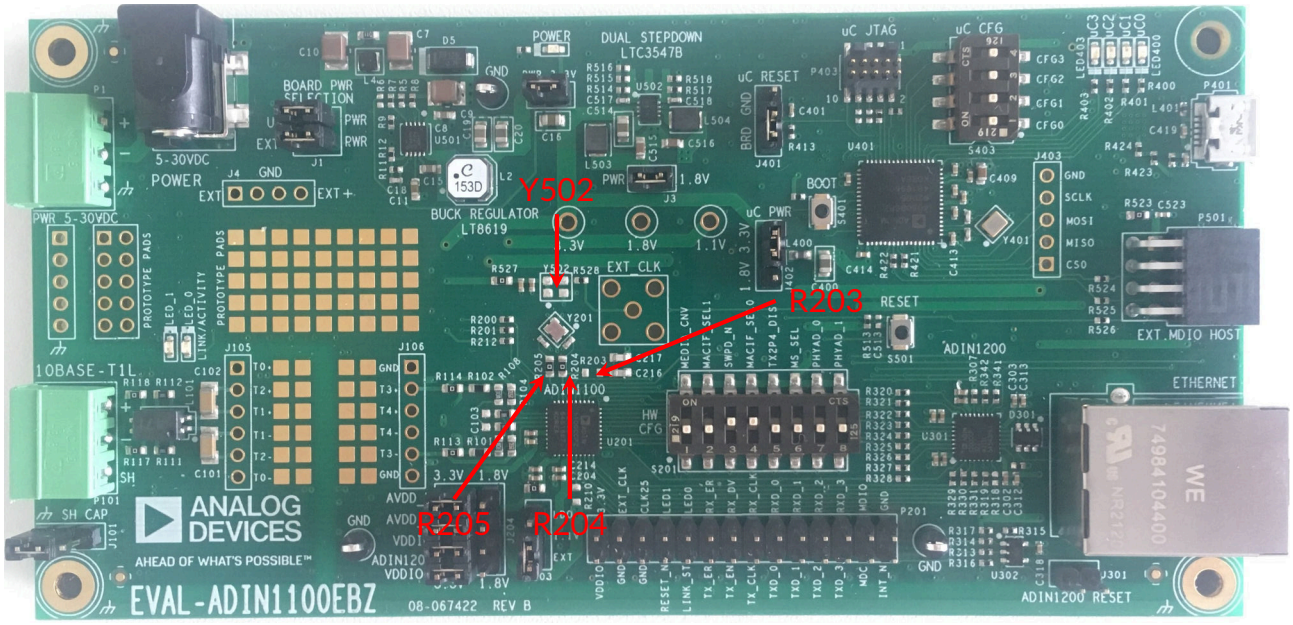

Figure 4: ADIN1100 evaluation board - components relevant for patching

2.2 RMII T1L Phy - Configuration

In order to configure the ADIN1100 evaluation board for attaching via RMII, the following steps should be followed:

- uC CFG switch selector, S403 - all positions to OFF
- uC RESET jumper, J401 - connected to the option GND, which means that the auxiliary microcontroller is held in reset
- uC PWR jumper, J402 - connected to the option 3.3V

- PWR 3.3V jumper, J2 (designator not shown in the silkscreen) - placed
- BOARD PWR SELECTION, J1 - both jumpers placed
- ADIN1100 POWER SELECTION, J204 - all jumpers placed to 3.3V
- ADIN1100 1.1V selector, J203 - placed in position EXT
- HW CFG (ADIN1100 HARDWARE CONFIGURATION) switch selector, S201 - configured as in Figure 5
- ADIN1200 RESET, J301 - placed

The configured board is shown below in Figure 5:

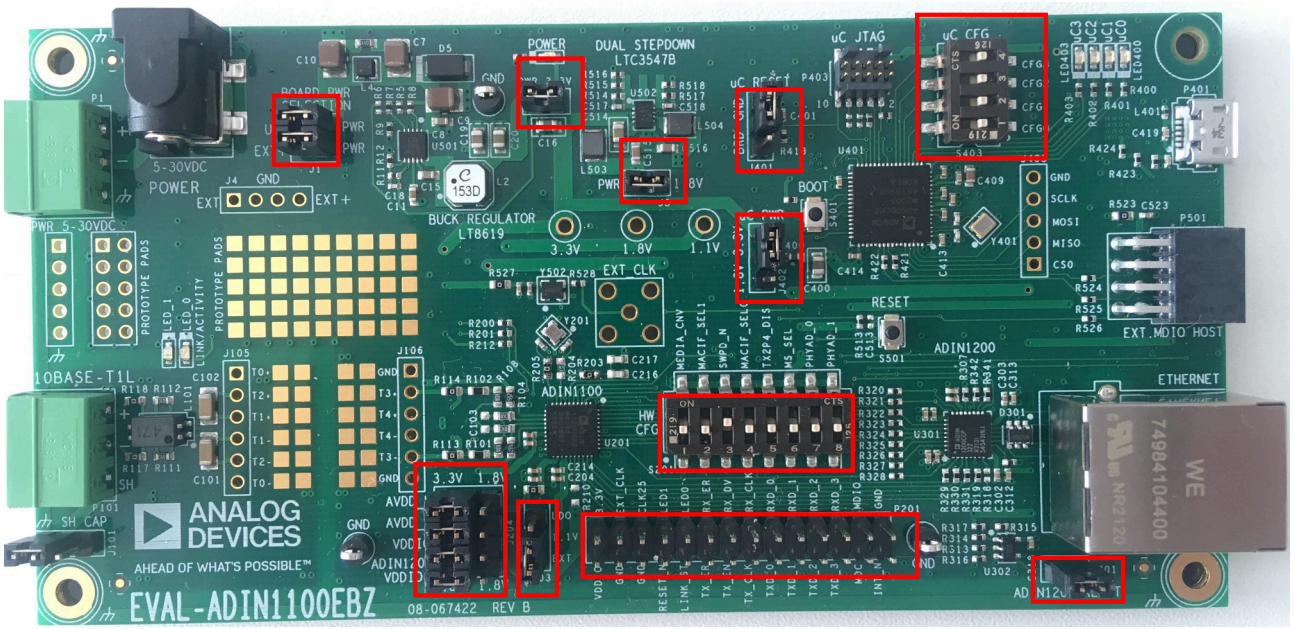

Figure 5: ADIN1100 evaluation board jumper/switch configuration

2.3 Media Converter - Configuration

In order to configure the ADIN1100 evaluation board as a 10BASE-T1L media converter board the following steps should be followed:

- In this setup, the power to the media converter will be supplied via P1. Other options could be via P2 or via P401 (USB). If P1 is used, a cable to the external power supply need to be prepared.
- uC CFG switch selector, S403 - all positions to OFF
- uC RESET jumper, J401 - connected to the option BRD
- uC PWR jumper, J402 - connected to the option 3.3V
- PWR 3.3V jumper, J2 (designator not shown in the silkscreen) - placed
- BOARD PWR SELECTION, J1 - both jumpers placed

- ADIN1100 POWER SELECTION, J204 - all jumpers placed to 3.3V
- ADIN1100 1.1V selector, J203 - placed in position EXT
- HW CFG (ADIN1100 HARDWARE CONFIGURATION) switch selector, S201 - configured as in Figure 6
- ADIN1200 RESET, J301 - not placed

In Figure 6 is shown the configured media converter board.

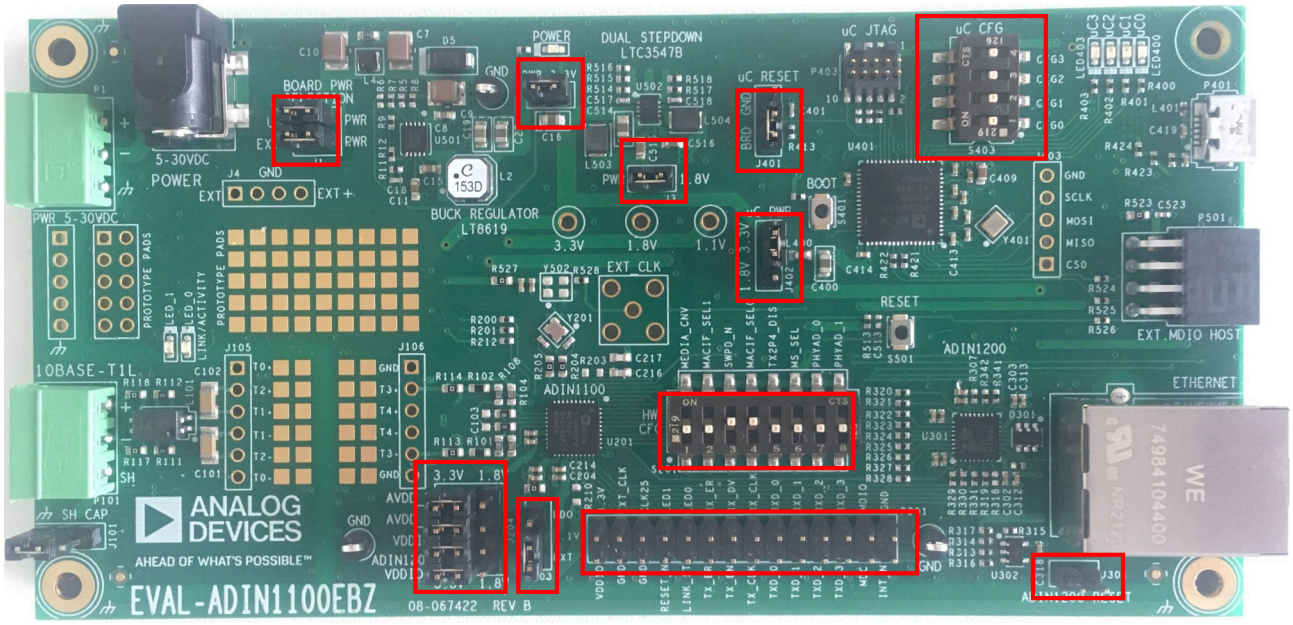

Figure 6: 10BASE-T1L Media Converter jumper/switch configuration

2.4 Setup preparation

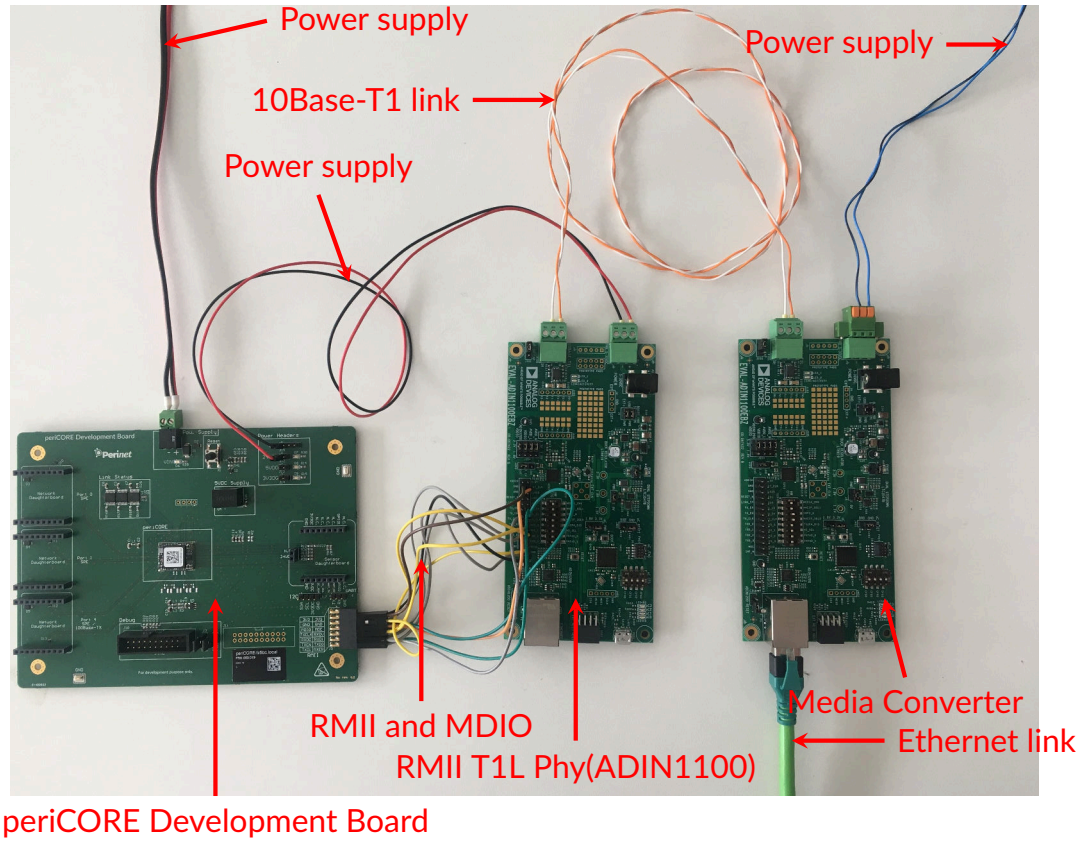

Figure 7: Hardware setup

An overview of the hardware setup is shown in Figure 7. The connections between the ADIN1100 evaluation board and the periCORE Development Board consists of the following signal groups: RMII, MDIO and the power supply.

2.4.1 RMII and MDIO Signals

RMII and MDIO signals are available on the headers J5 of the periCORE Development Board and P201 on the ADIN1100 evaluation board. The connections are given in the table below:

Signal Name	J5 pin[1]	J201 pin[2]
RX_ER	13	12
CRS_DV	7	14
TX_EN	12	13
TXD1	14	19
TXD0	11	17
RXD1	9	20
RXD0	10	18

Signal Name	J5 pin[1]	J201 pin[2]
REF_CLK	8 (TXCLK)	4 (EXT_CLK)
MDIO	6	26
MDC	5	25
GND	3	3
GND	4	5

Table 1: RMII and MDIO connections

The connections can be accomplished with short (10-15 cm) jumper cables as shown in Figure 7.

2.4.2 Power Supply

The ADIN1100 evaluation board will be supplied with 24 V from the periCORE Development Board. 24 V and GND are available on the headers J12 and J15, respectively. ADIN1100 evaluation board has two connectors, P1 and P2, for external power supply. In this application note, P1 will be used. The ADIN1100 evaluation board comes with the terminal block already plugged into P1. The terminal block has 3 screw terminals for: 24 V, GND and SHIELD. In the setup presented here (Figure 7), two jumper cables (for 24 V and GND) will be used with their female ends plugged into the headers J12 and J15 of the periCORE Development Board, while the other end of the cables will be screwed into the terminal block of the P1 connector on the ADIN1100 evaluation board.

2.4.3 Media Converter

The media converter board can be supplied with power via its connectors P1 and P2. In this setup, P1 was used and the board is directly powered from the 24 V power supply.

2.4.4 Network Cable

The link between the ADIN1100 evaluation board and the media converter is accomplished with a twisted wire pair. The 10BASE-T1L connector is available on P101 of each board.

[1] periCORE Development Board
[2] ADIN1100 evaluation board

3 Example periSTART-RMII-firmware

The periCORE communication module implements a multiport switch core. An additional PHY is connected via the reduced media independent interface (RMII), which is attached via its MAC at `PORT8` to the switch core (see Figure 8).

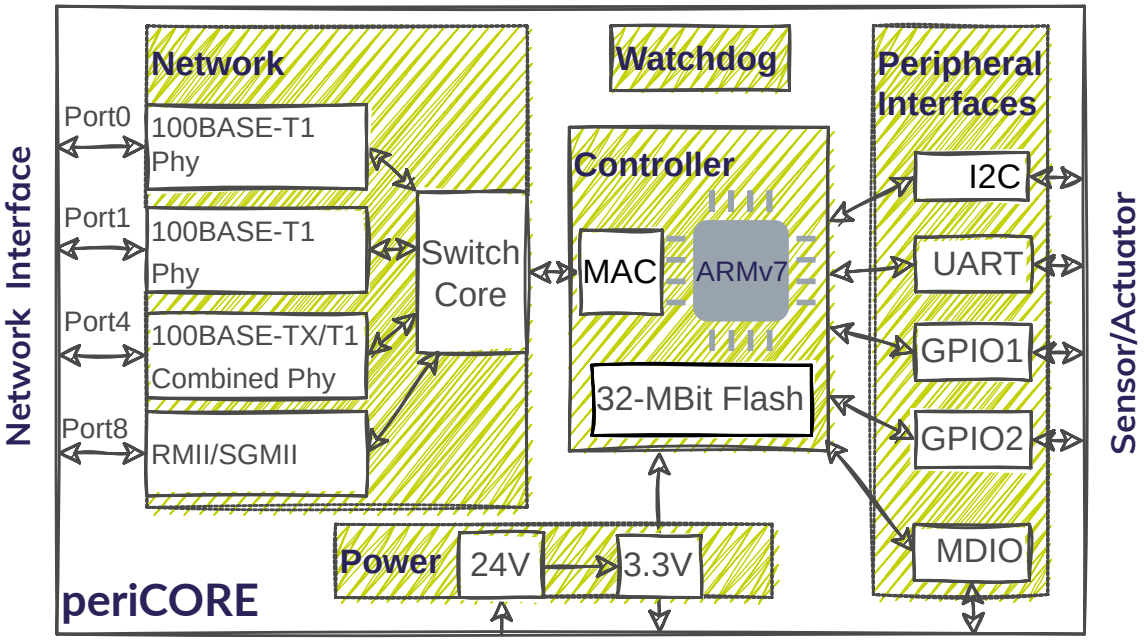

Figure 8: Block diagram of the periCORE module with its interfaces.

The firmware, periSTART-RMII-firmware [6], is provided as an example for operating the ADIN1100 T1L Single Pair Ethernet PHY with a periCORE communication module. It extends the periSTART-standard-firmware [7] and shows how to enable the RMII for `PORT8`:

- RMII Configuration
- Retrieve status information via MDIO interface.
- Provide link status information to the communication stack, for a flawless operation of the communication services.

A firmware implementation uses the libperiCORE C++API to perform the above-mentioned operations, further details are provided with the periCORE Datasheet [3].

3.1 RMII Configuration for `PORT8`

The provided C++-API provides a comfortable way to configure the network interface of the periCORE communication module. When constructing the libperiCORE runtime information `NodeEnvironment node_environment`, the default network configuration is provided as parameter.

```
//...
#include "version-info.h"
seve::System sevecore;
periCORE::NodeEnvironment node_environment{periCORE::switchcore::PERISTART};
// ADIN1100 device driver, phyaddress = 0x00
peripherals::ADIN1100 adin1100(0x00);
//...
```

Listing 1: Network Configuring as constructor parameter **src/main.cc**

The above excerpt, which can be found in the top of the file **src/main.cc**, shows that the NodeEnvironment is constructed with the `periCORE::switchcore::PERISTART` configuration. This configuration is a preset. It enables `PORT0` as 100BASE-T1 slave, `PORT1` as 100BASE-T1 master and `PORT4` as 100BASE-TX.

Note: The NodeEnvironment class will be constructed with the default network configuration `periCORE::switchcore::PERINODE` when the constructor parameter is omitted.

The following excerpt provides the preset configuration provided with the libperiCORE and is defined in the file **periCORE/switchcore/PortConfig.h**, which is delivered with the libperiCORE application development container.

```
//...
constexpr const PortConfig PERINODE = Port(PortID::PORT0, PortFlags::
    T1_SLAVE) + Port(PortID::PORT1, PortFlags::T1_MASTER);
constexpr const PortConfig PERICORE = PERINODE + Port(PORT4, PortFlags::
    TX);
constexpr const PortConfig PERISWITCH = PERINODE + Port(PORT4, PortFlags
    ::T1_MASTER);
constexpr const PortConfig PERISTART = PERICORE;
//...
```

Listing 2: Preset Network Configurations, **periCORE/switchcore/PortConfig.h**.

The network port `PORT8` is activated and configured inside the body of the applications `main` function. The following excerpt is taken from that function, which is defined in the file **src/-main.cc**.

```
//...
// update port8 configuration
node_environment.switchcore.port8.set_config(
    periCORE::switchcore::PortFlags::RMII_10BASE);
//...
```

Listing 3: Activate and configure `PORT8`. **src/main.cc**

The shown code line will configure the MAC of `PORT8` of the switch core as RMII in 10 Mbit full-duplex mode.

Note: The periCORE Network Interface configuration *must be* performed before start of the seveOS scheduler. With starting of the scheduler, the initialization sequence order cannot be maintained.

3.2 MDIO Interface Configuration

The periCORE provides access to the MDIO via the libperiCORE C++ API and can be accessed via `node_environment.peripherals.mdio`. The following excerpt provides an overview of the peripherals of the libperiCORE (`class NodeEnvironment`).

```
//...
// peripheral interface
struct
{
    // GPIO interface
    peripherals::GPIO& gpio1;
    peripherals::GPIO& gpio2;
    peripherals::GPIO& gpio3; // Note: shared with i2c SDA
    peripherals::GPIO& gpio4; // Note: shared with i2c SCL
    // peripheral interface for the UART
    peripherals::UART& uart;
    // I2C bus driver component, which receives i2c::Descriptors for data
    transfer.
    peripherals::I2C i2c;
    // peripheral interface for phy management
    // (Management Data Input/Output, MDIO)
    peripherals::MDIO& mdio;
} peripherals;
//...
```

Listing 4: C++ API for the MDIO interface. **libperiCORE/include/periCORE/NodeEnvironment.h**

The MDIO peripheral interface must be configured during initialization, before the seveOS scheduler is started. In the example firmware this is done inside the main function.

The MDIO peripheral interface is derived from a 31.25 MHz clock and by default disabled. The following excerpt shows how the communication speed of the MDIO device driver is configured to 2500kHz via the `set_clock(<speed>)` method. Configuring a value of `0` disables the MDIO peripheral interface.

In the second part, the ADIN1100 device driver implementation is connected to the MDIO bus driver. This allows the device driver to communicate MDIO frames to the ADIN1100-PHY.

```
//...
// update port8 configuration
node_environment.switchcore.port8.set_config(periCORE::switchcore::
    PortFlags::RMII_10BASE);
// enable and set MDC clock frequency to 2.5MHz
node_environment.peripherals.mdio.set_clock(2500 /*kHz*/);
// connect the out port of the ADIN1100 driver with the in port of the
    MDIO bus driver
adin1100.set_outport_mdio(node_environment.peripherals.mdio.get_inport());
// connect linkstatus change event
adin1100.set_outport_linkstatus_changed(node_environment.switchcore.port8
    .get_inport_linkstatus_changed());
//...
```

Listing 5: Activate MDIO and connect the ADNIN1100 device driver. **src/main.cc**

3.3 Forward PHY Link Status Information into the libperiCORE

The link status information of externally connected PHYs are not fetched automatically from the switch core, contrary to the native switch core ports (`PORT0`, `PORT1` and `PORT4`). Therefore, the link status event needs to be transported by software through the libperiCORE.

The ADIN1100 device driver fetches the status information from the PHY via MDIO. It provides an update to the libperiCORE via its outport `linkstatus_changed`. During the configuration phase the outport of the `ADIN1100` is connected to the inport of `port8` on the switch core. The `ADIN1100` emits at least one `linkstatus_changed` event in the beginning.

```
//...
// update port8 configuration
node_environment.switchcore.port8.set_config(periCORE::switchcore::
    PortFlags::RMII_10BASE);
// enable and set MDC clock frequency to 2.5MHz
node_environment.peripherals.mdio.set_clock(2500 /*kHz*/);
// connect the out port of the ADIN1100 driver with the in port of the
    MDIO bus driver
adin1100.set_outport_mdio(node_environment.peripherals.mdio.get_inport())
    ;
// connect linkstatus change event
adin1100.set_outport_linkstatus_changed(
    node_environment.switchcore.port8.get_inport_linkstatus_changed());
//...
```

Listing 6: Activate MDIO and connect the ADNIN1100 device driver. **src/main.cc**

3.4 ADIN1100 PHY Device Driver (MDIO)

The `ADIN1100` provides the device driver implementation. After the soft reset is done, the driver regularly (every 1s) reads the ADIN1100 Status Register. Its implementation fetches

the link status information via the MDIO interface.

On a changed status, it notifies the libperiCORE via its outport `linkstatus_changed`, which needs to be configured from the application (see Section 3.3).

```
//...
class ADIN1100
{
    using CL22RegisterAccessDescr = ::periCORE::peripherals::MDIO::
   CL22RegisterAccessDescr;

public:
    ADIN1100(unsigned char phy_addr);
    // set port to MDIO busdriver
    void set_outport_mdio(seve::eventflow::Sink<CL22RegisterAccessDescr
   *>* port);
    // set port to announce link status changed event
    void set_outport_linkstatus_changed(seve::eventflow::Sink<bool>* port
   ) { outport_lsc = port; }
private:
//...
};
```

Listing 7: The interface of the `ADNIN1100` device driver. **src/peripherals/ADIN1100.h**

The device driver uses the MDIO interface, attached to the outport `mdio`, to poll periodically the status of the hardware. The communication is done by preparing a register access descriptor `CL22RegisterAccessDescr`. Currently, only the Clause 22 MDIO frame format [8] compatible register access is implemented by the MDIO bus driver.

3.5 Retrieve Status Information via MDIO

The communication between the MDIO bus driver and the `ADIN1100` device driver is defined with the following class:

```
class CL22RegisterAccessDescr : public seve::lib::Chainable
{
public:
    CL22Frame frame{};
    seve::eventflow::Sink<CL22RegisterAccessDescr*>* done_port{nullptr};
};
```

Listing 8: Data structure for accessing the MDIO bus. **libperiCORE/include/periCORE/peripherals/MDIO.h**

This class has two members and they: describe what to do on the MDIO bus (command) and where to report that issued the command is finished. What to do on the bus is described with

the data structure called `CL22_Cmd`. This data structure represents a Clause 22 MDIO frame format [8]. Where to report that the issued command is finished is a pointer to an object of the Sink type (field named `done_port`) whose callback is called when the result of the MDIO command is assigned to it.

The data structure `CL22_Cmd` is shown below:

```
// clause 22 compatible frame
// +------+-+-+-+-+----+-----+--+--+----------------+
// | Bit: |0|1|2|3|4|...|8|9|...|13|14|15|16|.....|31|
// | 0    |                  preamble                |
// | 32   |sof|op |phy_a | reg_a | ta  |      data      |
// +------+-+-+-+-+----+-----+--+--+----------------+
struct CL22Frame
{
    enum OPCODE : uint32_t
    {
        WRITE = 1,
        READ = 2
    };
    enum : uint32_t
    {
        PREAMBLE = 0xFFFFFFFFUL
    };
    const uint32_t preamble = PREAMBLE;
    union
    {
        const uint32_t cmd_value = 0b01 << 30 /*sof*/ | 0b10 << 16 /*ta*/
   ;
        struct
        {
            uint32_t data : 16;    // 16-bit data field
            uint32_t ta : 2;       // turn around
            uint32_t reg_addr : 5; // register address
            uint32_t phy_addr : 5; // phy address
            OPCODE op : 2;         // operation identifier
            unsigned int sof : 2;  // start of frame
        } __attribute__((packed)) cmd;
    } __attribute__((packed));
} __attribute__((packed));
```

Listing 9: MDIO CLause 22 command data structure. **libperiCORE/include/periCORE/peripherals/MDIO.h**

The fields of the CL22_Cmd define:

op Operation code. This can be read or write

phy_addr address of the Phy to be accessed

reg_addr address of the Phy's register to be accessed

data stores the result of the read command or the data to be written in write command

ta turnaround time, defined in the MDIO bus specification. Default 0x02

4 Performance Measurements

The dashboard shows the live throughput of the periCORE, PORT1 (SPE), PORT4 (ETH) and PORT8 (RMII), (see Figure 9). The Dashboard is part of the integrated WebUI of the modified example `periSTART-RMII-firmware` [6].

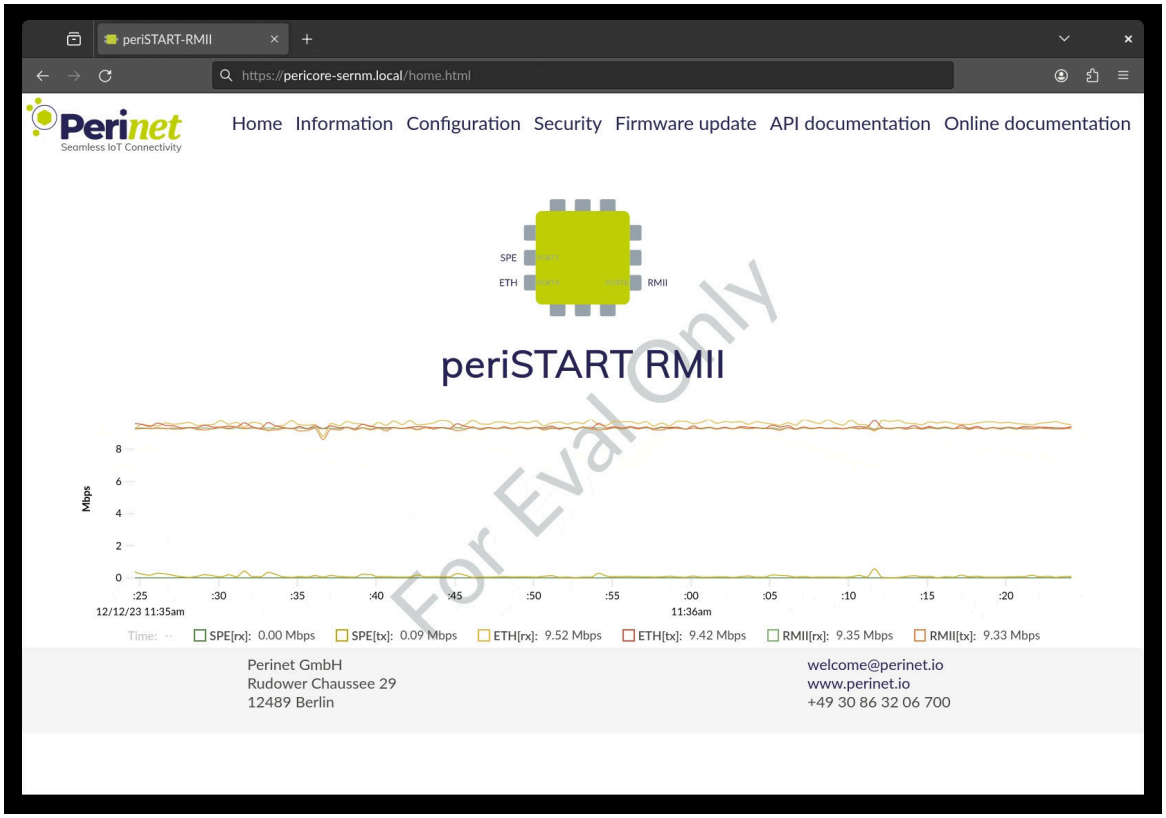

Figure 9: Performance dashboard WebUI.

4.1 Test Setup

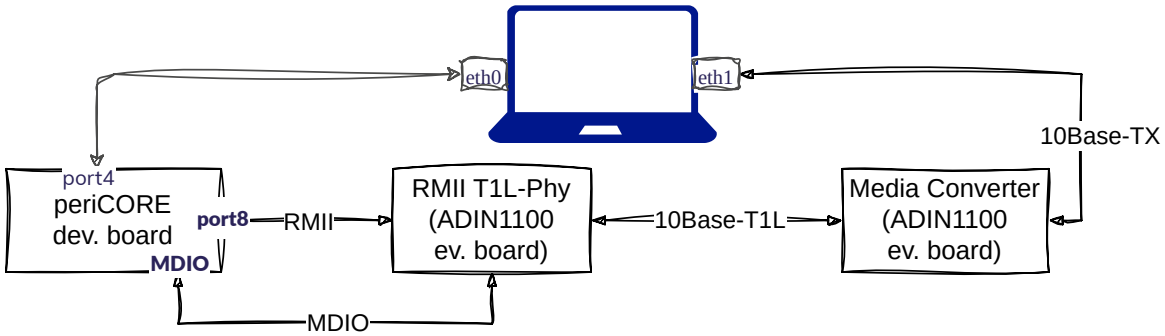

Figure 10: Simple Schematic of the Testsetup.

The periCORE Development Board is connected via its RMII interface to one of the EVAL-ADIN1100EBZ boards. In addition also the MDIO interface is connected.

4.2 Throughput Measurements

```
# server
iperf3 -6 --bind-dev eth0 -s

# client
iperf3 -6 --bind-dev eth1 -b 100Mb \
    -c fe80::9cef:a0de:5ae8:1db3 -t 120s \
    --bidir -P 3 --format Mbits --json \
    --logfile test.json --get-server-output \
    --extra-data "10BASE-T1L RMII periCORE Development Kit - EVAL-
   ADIN1100EBZ"
```

Listing 10: The iperf3 commands used during performance measurements.

Note: The option –bind-dev eth0 represents an Ethernet interface and fe80::9cef:a0de:5ae8:1db3 is its corresponding IPv6 LLA. Please note, the iperf3 client does communicate via a different Ethernet interface (eth1) to the IP address of the Ethernet interface eth0 in direct the traffic through the devices under test.

5 Ordering Information

Ordering Code	Product Name	Description
PRN.000.001	periCORE	periCORE single pair ethernet communication module.
PRN.000.019	periCORE Development Board	Minimal firmware development setup.
PRN.000.020	periCORE Development Kit	Full featured firmware development setup.

6 Contact & Support

For customer support, please call us at **+49 30 863 206 701** or send an e-mail to *support@perinet.io*.

For complete contact information visit us at www.perinet.io

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D Glossary

100BASE-T1 A Ethernet Standard where two endpoints are connected by a single twisted pair cable. It is one of the so-called Single Pair Ethernet (SPE) standards. It operates in full-duplex with a data rate of 100 MBit per second. Furthermore, it uses PAM-3 modulation with a voltage level from -1 to +1V, differentially on the two wires. 4

100BASE-TX A Ethernet Standard where two twisted pairs with differential signals are used, one for each direction. The data rate is 100 MBit per second. It is also called "Fast Ethernet". 4

10BASE-T1L A Ethernet physical layer standard (IEEE 802.3cg-2019) that was approved within IEEE on November 7, 2019. 10BASE-T1L core capability is a full duplex, dc balanced, point-to-point communication scheme with PAM 3 modulation at a 7.5 MBd symbol rate with 4B3T coding. It supports two amplitude modes: 2.4 V peak-to-peak up to 1000 m cable and 1.0 V peak-to-peak at a reduced distance. . 1, 4

MAC Media Access Controller, component that handles concurrent access to a shared physical communication medium. 12, 14

MDI Media Dependent Interface, a Fast-Ethernet chipset component. 4

MDIO Management Data Input/Output (MDIO), also known as Serial Management Interface (SMI) or Media Independent Interface Management (MIIM), is a serial bus defined for the Ethernet family of IEEE 802.3 standards for the Media Independent Interface, or MII. The MII connects Media Access Control (MAC) devices with Ethernet physical layer (PHY) circuits. The MAC device controlling the MDIO is called the Station Management Entity (SME). 6, 12, 14, 16

MII Media Independent Interface, a Fast-Ethernet chipset component. 4

PHY Physical layer. Lowest layer of the OSI model. 12, 15

RMII Reduced Media-Independent Interface, an interface defined as a standard interface to connect a media access control (MAC) block to an Ethernet physical transceiver chip . 1, 4, 6, 7, 12, 19

SGMII Serial Gigabit Media-Independent Interface, an interface defined as a standard interface to connect a media access control (MAC) block to an Ethernet physical transceiver chip . 4

E References

[1] Analog Devices. *Evaluating the ADIN1100 Robust, Industrial, Low Power 10BASE-T1L PHY*. Dec. 4, 2023. URL: https://www.analog.com/en/design-center/evaluation-hardware-and-software/evaluation-boards-kits/eval-adin1100.html.

[2] Analog Devices. *Robust, Industrial, Low Power 10BASE-T1L PHY*. Dec. 4, 2023. URL: https://www.analog.com/en/products/adin1100.html.

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F Revision History

Revision	Date	Author(s)	Description
1	2024-03-21	nsav,shoe	Initial Release